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# Suspension and measurement of graphene and Bi<sub>2</sub>Se<sub>3</sub> thin crystals

Jairo Velasco Jr, Zeng Zhao, Hang Zhang, Fenglin Wang, Zhiyong Wang, Philip Kratz, Lei Jing, Wenzhong Bao, Jing Shi and Chun Ning Lau

Department of Physics and Astronomy, University of California, Riverside, CA 92521, USA

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## Abstract

Coupling high-quality suspended atomic membranes to specialized electrodes enables the investigation of many novel phenomena, such as spin or Cooper pair transport in these two-dimensional systems. However, many electrode materials are not stable in the acids that are used to dissolve underlying substrates. Here we present a versatile and powerful multilevel lithographical technique to suspend thin crystals, which can be applied to the vast majority of substrate, crystal and electrode materials. Using this technique, we fabricated suspended graphene devices with Al electrodes and a mobility of  $5500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . We also demonstrate, for the first time, fabrication and measurement of a free-standing thin Bi<sub>2</sub>Se<sub>3</sub> crystal, which has low contact resistance to electrodes and a mobility of  $\gtrsim 580 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ .

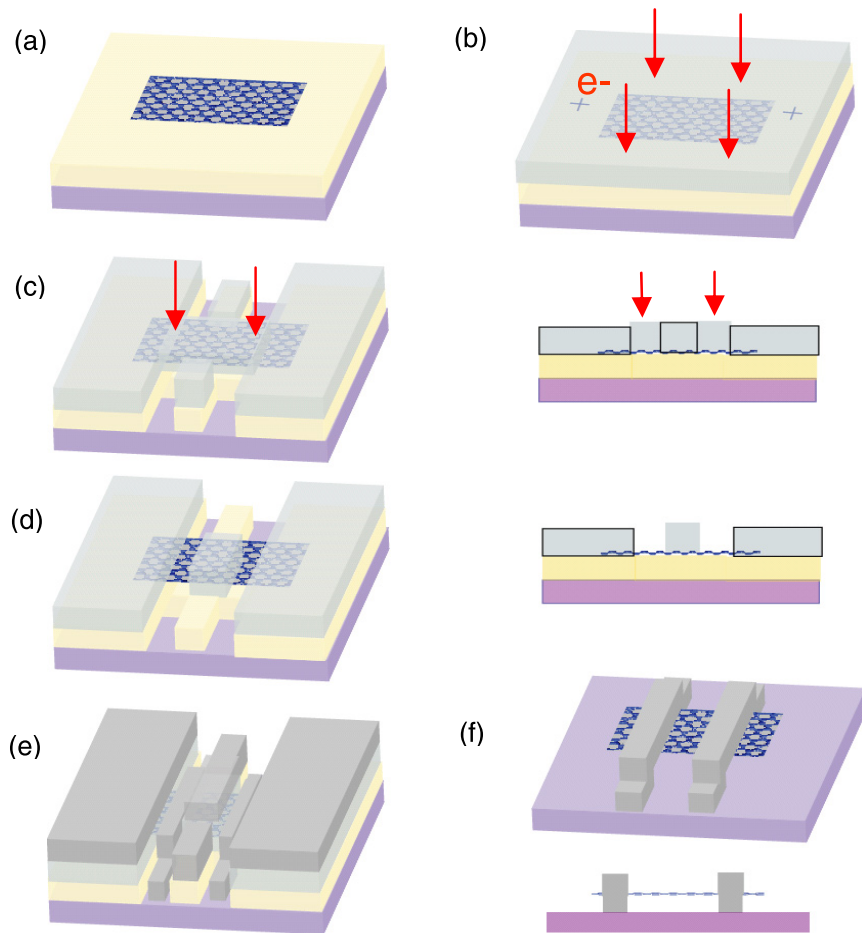
(Some figures in this article are in colour only in the electronic version)

Recently, thin crystals (TC) that are extracted from layered materials have become popular platforms for the investigation of novel physical phenomena [1]. Some of the most studied materials are thin sheets of graphite [2], Bi<sub>2</sub>Se<sub>3</sub> and Bi<sub>2</sub>Te<sub>3</sub>, which provide platforms for investigating massless Dirac fermions [3, 4] and topological insulators [5–7]. Due to their two-dimensionality, they display a number of desirable characteristics such as gate tunable charge density and/or type, enhanced Coulomb interaction and coupling between local morphology and electronic properties [8, 9]. As surface 2D electron systems, these membranes also enable optical and scanned probe measurements that are not possible in traditional semiconductor heterostructure devices.

Another significant advantage of these systems is that they can be easily coupled to special electrodes, such as superconductors or ferromagnets, potentially enabling the experimental realization of some of the most fascinating predictions for these systems, such as specular Andreev reflection [10], Majorana fermions [11, 12] and the spin Hall effect. Yet, interaction between the TC and the substrate is known to be a significant impediment to the observation of such phenomena, since the substrate can locally dope the membranes, induce local corrugations and strains, and introduce scatterers such as charged impurities and surface phonons. Thus far, removing the substrate has proven to

yield exceedingly high-quality devices [13, 14], yielding novel phenomena such as Wigner crystallization and Mott insulating states in carbon nanotubes [18, 19] and fractional quantum Hall effect in graphene [20, 21].

The most commonly adopted technique for removing substrates is acid etching [13–15], which dissolves the oxide layer underneath the device. However, this technique suffers from several drawbacks, including limitation of membrane and electrode materials to those that are stable in acid, and substrate to those that are not. For instance, superconducting and ferromagnetic materials cannot survive such a procedure and many of the much sought after topological insulator materials, including Bi<sub>2</sub>Se<sub>3</sub> and Bi<sub>2</sub>Te<sub>3</sub>, are also partially soluble in hydrofluoric acid that etches SiO<sub>2</sub>. Here we report an innovative multilevel lithography technique to fabricate devices with free-standing TC extracted from layered materials. Employing only standard resists and developers for lift-off lithography, this technique can be applied to the vast majority of commonly used substrate, crystal and electrode materials, while imparting minimal damage to the device, which does not undergo any acid etching. Moreover, since the device is suspended above the substrate, the risk of gate leakage is minimized. Using this technique, we demonstrate the fabrication of free-standing graphene coupled to Ti/Al electrodes, with a number of widths and source–drain



**Figure 1.** Three-dimensional schematics of the fabrication process. Side views of the process are also shown in parts (c), (d) and (f). (a) TC is exfoliated onto LOR (yellow) which rests on the SiO<sub>2</sub>/Si substrate (purple). (b) Bilayer MMA/PMMA (light gray) resists are deposited onto the sample, and alignment cross marks are patterned by EBL. A second EBL procedure is performed to expose regions indicated by the red arrows. (c) Development in MIBK and MF319 removes both LOR and the MMA/PMMA bilayer in the exposed regions. The final EBL step is performed to expose regions indicated by the red arrows. (d) Development in MIBK removes only the MMA/PMMA resist bilayer in the exposed regions. (e) Metal deposition is performed at +45°, -45° and 0° using Ti/Al (dark gray). Samples are then immersed in warm Remover PG and dried using a critical point dryer, leaving suspended electrodes that ‘hold’ AM above the substrate.

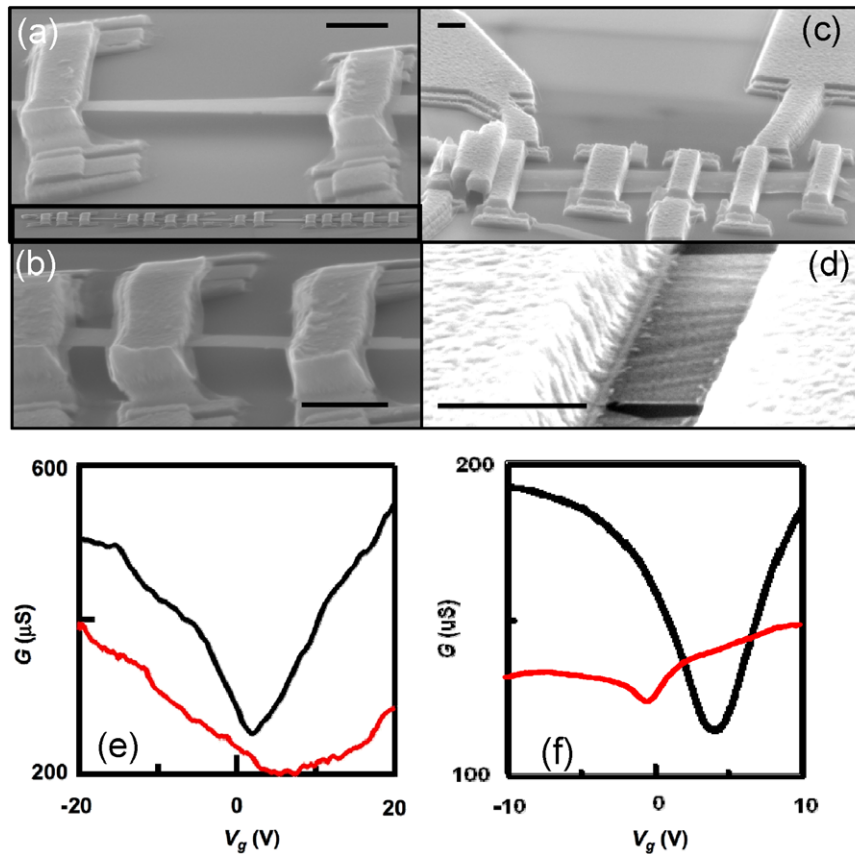
separations. We also report, for the first time, fabrication and measurement of suspended thin Bi<sub>2</sub>Se<sub>3</sub> membranes (~65 nm), with an estimated mobility of  $\sim 500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . In the future, this versatile technique could be used to explore, for instance, superconductivity and spintronics in high mobility graphene and Bi<sub>2</sub>Se<sub>3</sub> samples, as well as in other layered materials.

This fabrication process is based on a method developed by us [22] to suspend local gates above graphene. The procedure, which consists of three electron beam lithography (EBL) steps, utilizes the different exposure, development and lift off properties of different resists. Figure 1 illustrates the entire procedure for creating two suspended electrodes that contact a free-standing membrane. In the first step, we deposit and bake a layer of lift-off (LOR) resist onto a p-doped Si chip that is covered with a 310 nm thick SiO<sub>2</sub> layer. TC sheets are directly exfoliated onto the LOR layer, and can be identified using an atomic force microscope or color interference under an optical microscope (figure 1(a)). Subsequently, a bilayer of electron beam resists, methyl methacrylate/poly(methyl methacrylate) (MMA/PMMA), are spun and baked onto the sample, followed by exposure of

alignment mark patterns and development in methyl isobutyl ketone (MIBK). These alignment marks are used for locating and aligning electrode patterns to the TC in the subsequent steps. We note that no metal deposition is necessary, as openings in the PMMA/MMA layer are sufficiently visible in the scanning electron microscope (SEM) for alignment, thus greatly simplifying the fabrication procedure.

In the next step, we use EBL to expose areas adjacent to the TC, and develop in MIBK/isopropyl alcohol (IPA) solution that dissolves only the exposed regions of the MMA/PMMA bilayer but not LOR, so that two windows in the resist bilayer are created on either side of the TC. The exposed LOR within the windows is removed by developing in MF319, while the rest of the LOR layer remains intact (figure 1(c)). The end result of this step is four windows on the LOR/MMA/PMMA resist, which, after metallization, will form anchors on the substrate to connect to and support the two suspended electrodes.

In the third and final step of fabrication, we fabricate two suspended electrodes to contact the TC. To this end, we expose two long rectangular windows that lie directly on top



**Figure 2.** SEM images and transport data for suspended graphene devices. (a)–(d) SEM images of suspended graphene sheets with different widths and lengths. Scale bars: 1 μm. Inset: a 40 μm long graphene sheet suspended by several electrodes. (e), (f) Device conductance as a function of gate voltage for two different suspended graphene devices. Red and black traces are for as-fabricated and current-annealed devices, respectively.

of the TC and connect to the openings created in step 2 (figure 1(d)). The chip is developed in MIBK/IPA to remove the exposed MMA/PMMA. We then perform metal deposition at three different angles (+45°, −45° and 0°) to ensure good contact at the sidewalls that attach the anchors to the suspended electrodes [23]. Finally, the samples are immersed in warm Remover PG to remove all the resist layers, and dried using a critical point dryer to prevent structural instability during the drying process. The end result is a sheet of thin crystal ‘held up’ by two partially suspended electrodes.

This powerful fabrication technique is versatile and robust. By tuning lithography parameters, we can produce free-standing electrodes that suspend layered materials with varying widths, lengths and heights. Using graphene as an example of a TC, we fabricated a number of suspended devices with electrode separations ranging from 700 nm to 4 μm (figure 2), with a total suspended length as long as 40 μm (figure 2(a) inset). The graphene sheets usually exhibit no discernible structural deformation, though strain-induced ripples [24] have been occasionally observed (figure 2(d)). In these examples, graphene sheets are suspended at ~300 nm above the SiO<sub>2</sub> substrate, though this height can be easily adjusted from 50 nm to 3 μm by selecting different LOR solutions.

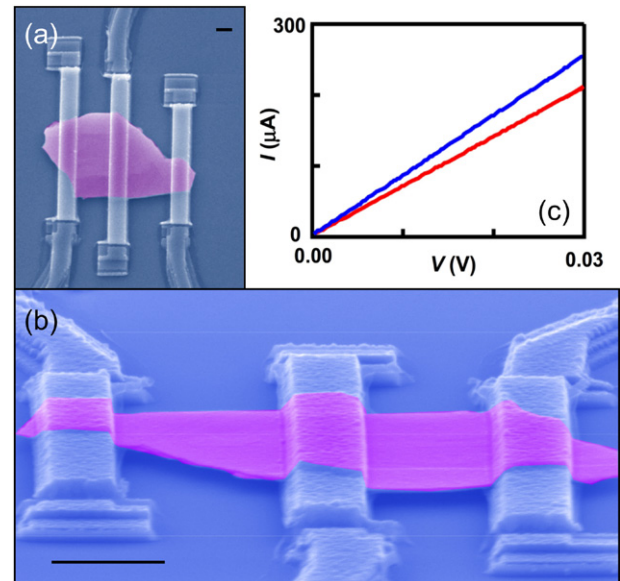
This acid-free fabrication technique is capable of producing devices with both long and short electrode

separations. The latter geometry is particularly interesting for realization of a ballistic graphene-based Josephson junction for example. Such a system has been predicted to exhibit several novel phenomena, such as specular Andreev reflection [25], chargeless transfer of spins [26] and thermopower [27], but has yet to be experimentally realized.

To demonstrate the viability of this fabrication procedure, we fabricate free-standing graphene devices with Ti/Al electrodes, and measure their transport characteristics using standard lock-in techniques at low temperature. In figures 2(e) and (f) we plot the conductance  $G$  as a function of gate voltage  $V_g$  for two different devices similar to the ones shown in figures 2(c) and (d). The data displayed in figure 2(e) were obtained from a device with a source–drain separation of 1.7 μm, and graphene width 3.5 μm. The red trace shows the device’s initial  $G(V_g)$  behavior immediately after fabrication. The relatively large conductance indicates small contact resistance; however, the poor response to gate and the absence of a Dirac point suggests that the device is highly doped. Such behavior is not uncommon for as-fabricated suspended graphene devices. After current annealing [13, 14, 28] at ~1.2 mA for 10 min, the device’s behavior is significantly improved. As shown by the black trace, the Dirac point appears at  $V_g \sim 0$ , and the  $G(V_g)$  is symmetric with respect to the electron and hole branches. The device mobility is estimated to

be  $\sim 3000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which is reasonable and can be further optimized. The reproducibility of the results is demonstrated by similar behavior from a second device, with a mobility of  $5500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  (figure 2(f)). This measured mobility value is lower than that reported previously for suspended graphene devices [13, 14, 16, 17], and is probably due to contamination incurred during critical point drying, since liquid  $\text{CO}_2$  is known to be a good organic solvent. In future studies, this could be remedied by using high purity liquid  $\text{CO}_2$  or switching to a solvent-only drying technique [13]. The device's gate coupling efficiency can be estimated from the parallel-plate capacitance between the back gate and graphene, which are separated by 310 nm of  $\text{SiO}_2$  and 300 nm of vacuum. We note that a  $V_g$  of up to 80 V can be applied (or equivalently, an induced charge density up to  $1.2 \times 10^{12} \text{ cm}^{-2}$ ) without collapsing graphene, which is approximately an order-of-magnitude higher than that applied to free-standing graphene devices fabricated via acid release of  $\text{SiO}_2$  [13, 14], thus allowing access to regimes of high carrier density with rich many-body effects.

As a further demonstration of the versatility of this procedure, we fabricated suspended  $\text{Bi}_2\text{Se}_3$  membranes, which is also a layered material. This topological insulator material is predicted to have a plethora of fascinating physical phenomena [7, 29]. Experimentally, the most illuminating results to date arise from data obtained from angle-resolved photoemission spectroscopy and scanning tunneling microscope measurements [30–32], while transport measurements have been limited [33, 34]. Here we demonstrate the fabrication and measurement of suspended  $\text{Bi}_2\text{Se}_3$  membranes, which have not been reported previously. The bulk samples are synthesized via Ca doping of single crystal  $\text{Bi}_2\text{Se}_3$  crystals [35]. Figures 3(a) and (b) display SEM images of a completed  $\text{Bi}_2\text{Se}_3$  device, which was measured by atomic force microscopy to be  $\sim 65 \text{ nm}$  thick. The current–voltage ( $I$ – $V$ ) characteristics of this device at 300 K and 4 K are both linear, with resistances of 142 and  $117 \Omega$ , respectively (figure 3(c)). The linear  $I$ – $V$  curves, in addition to the relatively small resistance that decreases with temperature, indicate low contact resistance and metallic conduction. Additionally, we also observed a small gate dependence: application of  $\Delta V_g = 5 \text{ V}$  induces a  $\sim 10 \mu\text{S}$  change in conductance (5% change), suggesting that while much of the current is transported through the bulk there could be some surface conduction. Assuming parallel conduction through the surface states and the bulk [36], and that the charge density of the bulk is not affected by  $V_g$ , we estimate the field effect mobility  $\mu_s$  of the device's surface state by  $\Delta G = (W/L)\Delta n_s e \mu_s = \alpha(W/L)\Delta V_g e \mu_s$ , where  $\alpha = 1.5 \times 10^{10} \text{ cm}^{-2}$  is the gate coupling efficiency,  $W/L$  the device's aspect ratio, and  $e$  the electron charge. Using  $\Delta V_g = 5 \text{ V}$ ,  $W/L = 0.7$  and  $\Delta G = 10 \mu\text{S}$ , we obtain  $\mu_s \sim 580 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . This simple calculation ignores the possible difference in gate response for the top and bottom surface states, but could serve as an order-of-magnitude benchmark for sample quality. In the future, we expect that the device can be further optimized via improvement in material quality and reduction in membrane thickness.



**Figure 3.** SEM images and transport data of a suspended  $\text{Bi}_2\text{Se}_3$  device. (a), (b) Top and angled view of a suspended  $\text{Bi}_2\text{Se}_3$  device. Scale bar:  $1 \mu\text{m}$ . The images are false-colored. (c) Current measured as a function of voltage bias at 300 K (red) and 4 K (blue).

In conclusion, we have developed a gentle and versatile multilevel lithography process to fabricate free-standing thin crystals that are extracted from layered materials. Using this technique, we successfully suspended and performed measurements on atomically thin graphite and  $\text{Bi}_2\text{Se}_3$  films that were coupled to Ti/Al electrodes. This technique provides a viable path toward the investigation of induced superconductivity and spintronics in high mobility graphene and  $\text{Bi}_2\text{Se}_3$  samples, as well as in other layered materials.

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